Wafer-edge yield engineering in leading-edge DRAM manufacturing

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**Introduction**

In today’s business climate, continuous innovation and productivity improvements are essential to the survival of any company. In the semiconductor industry, productivity improvement is generally accomplished using decreased cost-per-function, economy of scale, increased wafer diameter, process simplification and yield enhancement. The challenges for extreme edge dies increased with the conversion from 200mm to 300mm wafer processing, and will be further increased by the transition to 450mm [3]. Increasingly sophisticated and more expensive equipment is required for technology shrinks, making the acquisition of funds for capacity expansion ever more difficult. Process simplification can only be done to a certain extent. Emphasis is therefore placed on fast yield learning, which claims the biggest financial leverage. Due to the narrower process windows at smaller technology nodes, center-to-edge uniformity over the wafer is crucial for yield [4]. Consequently, wafer-edge and bevel-induced yield loss were introduced as critical elements to the International Technology Roadmap for Semiconductors (ITRS) in 2005 and are still considered challenging [5, 6]. The ITRS also highlights the importance of rim problems in the wafer-edge exclusion guideline.

A recent report described the economically optimized technology transfer and ramp methodology from development to a mass-production site within a global fabrication cluster [7]. This paper outlines the wafer-edge yield engineering methodology, which was essential for the reported steep production ramp.

**Wafer edge-specific process issues**

Several factors can cause considerable yield loss, factors that include non-uniformities in film thickness and etch profiles due to plasma inhomogeneity towards wafer edge; wafer bow due to film stress; residues at bevel and backside; chuck damage by reactive gases or particles; and plasma- or handling-induced mechanical damage at bevel. Two examples of wafer edge-specific issues at early development phase are depicted in Figure 1. The Scanning Electron Microscope (SEM) cross-section shows distorted oxide hard mask patterns and an optical microscope image reveals chipping during deep-trench (DT) structuring.

Statistical data for regional yields for 80nm DRAM technology at premature stages are shown in Figure 2. Regions with identical chip count are defined concentrically from the wafer center (region A) towards wafer edge (region E). Obviously, the yield at wafer edge is the lowest. Regions A to D are at a comparable high level indicating better process uniformity and controllability.

**Overkill at wafer edge**

For wafer-edge detractors, electrical failure analysis can provide only limited information due to superposition of process issues from more layers compared to wafer center. Extensive reverse engineering is required, especially if process issues or defects are non-detectable inline. Additional delays are caused if analysis has to be carried.
out in serial mode, in a similar fashion to archaeological digs uncovering the buried achievements of ancient civilizations layer by layer. Figure 3 shows an example of debugging of multiple process issues at an edge die.

Initially, only the cluster bitline fail was observed electrically; physical failure analysis indicated that it was due to a local contact-to-bitline (C1-M0) overlay shift. Within the affected die no overlay shift was present towards wafer center. Statistical analysis confirmed a baseline issue for the given die which, once fixed by appropriate overlay correction, showed failures in master data lines (MDQ) in the electrical fail signature. Physical failure analysis revealed that the observed MDQ fail was associated with back-end-of-line metallization contact (C2) opens. The defects were optically non-visible by inline defect inspection. Hence, a voltage contrast-based e-Beam defect inspection was developed for inline monitoring, while the issue was addressed using blading adjustment for the extreme edge shot [8]. Finally, single cell fails were detected, caused by a localized active-area to deep-trench capacitor (AA-DT) overlay shift at the extreme edge of the affected die. The cause of these fails could be attributed to shifted DTs due to plasma distortion during hard-mask open process. Eventually, the process uniformity could be further optimized by a redesign of the etch tool. Learning cycles could be further reduced by use of the Automated Process Inspection (API) feature of the SEM review tool [9]. A specifically designed API recipe provided inline information on AA/DT overlay shift right after AA etch in this case, which negated the need for waiting for the electrical test to verify the process fix.

Bevel engineering

There are various possible methods of addressing wafer-edge issues, including widening the process windows, centering the process windows, improving the process uniformity, or centering the process window differently at center and edge as depicted in Figure 4. Process non-uniformities within the specified process window lead to a good die. In addition to process non-uniformities, defects originating from wafer bevel become increasingly important for overall yield improvement. In the near future, bevel treatment and inspection tools will be an integral part of the standard process flow [10]. Bevel defects can be transferred to the active wafer surface by subsequent process steps; in particular, bench-type wet clean tools can be prone to transfer bevel defects. Single-wafer cleaning tools where the cleaning chemistry is injected at the center of the rotating wafer do not suffer from such a tendency; however, this advantage is balanced out by the drawback of the tools’ higher cost of ownership.

Cross-contamination via etch or deposition due to plasma attack or
thermal stress-induced delamination cannot be ruled out even if a single wafer cleaning tool is used. If wafer-edge exclusion is already optimized, other means such as bevel polish or bevel etch are needed to overcome cross-contamination issues. The production process of 90nm and 80nm DRAM products in this study showed needle-shaped defects, which turned out to be poly-silicon residues from the bevel area as shown in Figure 5. Such residues could be successfully removed by bevel dry etch – which has not been benchmarked with bevel polish in the present case, bevel wet etch, bevel plasma etch, and bevel brush clean tools which are also available commercially.

Yield test chip

Yield Test Chips (YTCs) are effective tools for identifying process windows, especially during technology development [11], and also provide a useful yield management methodology for hard-failing dies at wafer edge. Hard fails are found during basic functional tests and indicate issues like shorts and opens. The proprietary YTC uses a special mask set that is incorporated in the standard process flow. Each reticle shot of the YTC design consists of plain product chips and two different kinds of test chips. Both test chip types consist mainly of comb and meander structures to probe process sequences for shorts, opens, and process windows for critical dimensions and overlay. In the first test chip type, all test structures have their own probe pads, while in the second, huge arrays of similar test structures are
connected using bitlines and wordlines
with probe pads at array edge only. The
major advantage of the second type
is that the number of contact pads is
largely reduced, thus leading to smaller
test structures that allow better failure
localization.

A good example of a successful
YTC application is a process issue at
‘three o’clock’ wafer location as shown
in Figure 6. A strong response is noted
for a fail rate related to misalignment
of periphery bitline contacts to active
area (CG/CS-AA). A similar response
was also seen for bitline (M0) opens,
whereas no correlation was found for
other process parameters. Engineering
efforts were needed to focus on those
two process sequences.

A disadvantage of the YTC is its need
for a new design of a complete mask
set and an appropriate test capability,
making it costly and time consuming.

A so-called Test Sequence Limited
Yield (TSLY) test chip was developed
for analysis of soft fails, which occur
during test of chip functionality for
specified temperature, voltage, and
timing ranges. The TSLY approach was
less costly than the previous approach
as only one front-end-of-line mask
required modification, which was
identified by the YTC as the layer with
the biggest yield opportunity. Only the
critical dimensions of DRAM product
were varied in this instance; standard test
could be used for fast electrical analysis.
The influence of DT top dimensions on
the retention performance (S12_SP) is
shown in Figure 7, which demonstrates
that better retention performance
is obtained for increased DT length
(DTL) and reduced DT width (DTW).

**Inline monitoring strategy**

In volume production, the sampling
for metrology and line monitoring
is carefully optimized for a high
throughput and to allow the detection
of any excursion in good time. Initially,
the throughput-optimized standard
sampling frequency and number of
measurement points were found to be
insufficient for wafer-edge learning
and required the implementation of a
special monitoring route with adapted
sampling and additional measurement
points. Special recipes such as voltage
contrast-based e-Beam inspection
and API were adapted for subsequent
technologies from the beginning, thus
allowing for issues to be tackled in
parallel mode.
Team setup and progress tracking

An essential precondition for fast wafer-edge yield learning is the allocation of dedicated resources at an early stage. One cross-functional team with experts from process integration, product engineering, physical failure analysis, unit process, metrology, and defect density engineering co-worked on wafer edge and level topics for this particular study. Regular information exchange within the Qimonda fabrication cluster assured fast knowledge transfer between the sites. Key process indicators such as hard and soft fail yields were defined with automatic data collection, by which process modifications could be easily assessed for wafer edge dies. A joint improvement roadmap was defined for the globally distributed manufacturing sites.

The improvement of wafer-edge yield impact is compared for the 90nm production ramp in Figure 8, from which it is apparent that learning speed for wafer edge yield could be more than doubled for the 75nm technology.

Conclusion

Yield learning speed at wafer edge was improved using a new methodology for sub-90nm DRAM technologies in this particular study. While for 90nm technology, fixing edge detractors took time because the topics were not visible, with the standard setup, the learning speed for 80nm and 75nm could be significantly improved by application of a new approach. The key contributors to the technology’s success were the dedicated cross-functional team, a modified metrology setup, specific inspection recipes, and new process tools. In addition, two kinds of test chips were used to identify the root cause for soft and hard fails, and possible routes for debugging multiple process issues were presented. Best practice sharing within the fabrication cluster supported an aggressive global production ramp.

ACKNOWLEDGEMENTS

The authors would like to extend special thanks to the members of the global wafer edge improvement team for their relentless efforts.

REFERENCES


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